REMARKS

This paper is presented in response to the Office Action. By this paper, claims 1, 14, and 25 are amended and no claims are added or cancelled. Claims 1-30 remain pending.

Reconsideration of the application is respectfully requested in view of the following remarks. For the convenience and reference of the Examiner, Applicants' remarks are presented in the order in which the corresponding issues were raised in the Office Action.

I. General Considerations

a. claim amendments and/or cancellations

Applicants submit that none of the claim amendments, claim cancellations or statements that have been, or may be, advanced by the Applicants in this or any related case, constitute or should be construed as, an implicit or explicit surrender or disclaimer of claim scope with respect to the cited, or any other, references.

b. remarks

Applicants respectfully note that the remarks herein do not constitute, nor are they intended to be, an exhaustive enumeration of the patentable distinctions between any cited references and the invention, example embodiments of which are set forth in the claims of this application. Rather, and in consideration of the fact that various factors make it impractical to enumerate all the patentable distinctions between the invention and the cited art, as well as the fact that the Applicants has broad discretion in terms of the identification and consideration of the base(s) upon which the claims distinguish over the cited references, the distinctions identified and discussed herein are presented solely by way of example. Consistent with the foregoing, the discussion herein is not intended, and should not be construed, to prejudice or foreclose contemporaneous or future consideration by the Applicants, in this case or any other, of: additional or alternative distinctions between the invention and the cited references; and/or, the merits of additional or alternative arguments.

Applicants note as well that the remarks, or a lack of remarks, set forth herein are not intended to constitute, and should not be construed as, an acquiescence, on the part of the Applicants: as to the purported teachings or prior art status of the cited references; as to the characterization of the cited references advanced by the Examiner; or as to any other assertions, allegations or characterizations made by the Examiner at any time in this case. Applicants

reserve the right to challenge the purported teachings and purported prior art status of the cited references at any appropriate time.

II. Claim Rejections under 35 USC § 102 only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Further, the identical invention must be shown in as complete detail as is contained in the claim. Finally, the elements must be arranged as required by the claim. *Manual of Patent Examining Procedure ("MPEP") § 2131.*

Turning now to the Office Action, the Examiner has rejected claims 1-7, 13-20, 25-27 and 30 (claims 1, 14 and 25 are the pending independent claims) under 35 U.S.C. § 102(b) in view of US 5,850,422 to Chen ("*Chen*"). For at least the reasons set forth below, Applicants respectfully disagree.

a. claims 1-7 and 13

As noted above, Applicants have amended claim 1 to further distinguish over the cited art. As amended, claim 1 recites that the first and second clock signals are received from a source other than one of the plurality of circuit elements. Further, claim 1 recites that the selector receives as input separate data signals from the plurality of circuit elements and then generates an output signal that includes the received data signals. Support for such amendments is found at least in the originally filed specification at Figures 3-7 and their accompanying text.

Chen, in sharp contrast, does not teach a multiplexing circuit as recited in amended claim 1. For example, the Examiner has alleged that the selector recited in claim 1 corresponds to element 16 or 52 of *Chen*. Accordingly, the only elements of *Chen* that can reasonably correspond to the plurality of circuit elements that each provide a signal to the mux 16 are elements 12, 14, and 20 as they are the only elements that provide a signal to the mux 16. However, nowhere does *Chen* teach or suggest that that any of these elements is clocked by a first clock signal that is received from a source other than one of the plurality of circuit elements. In fact, at best *Chen* teaches that a phased lock loop 12 provides clock signals to the data sampler 14 and to the clock mux 16 that are recovered by the mux 16. Thus, Chen does not teach or this element of claim 1.

Applicants note further that the Examiner has alleged that "...Chen discloses a circuit...for multiplexing a plurality of data signals (36)..." However, the passages cited by the Examiner do not appear to recite the multiplexing of data signals.

As well, Applicants note that the Examiner has referred to *Chen* as disclosing a "...first clock signal substantially in-phase with said transition..." and a "second clock signal." *Office Action* at 2-3. However, it is not clear to Applicants which portion(s) of *Chen* the Examiner believes to constitute such "first clock signal" and "second clock signal." Bearing in mind the other characterizations advanced by the Examiner, it would seem that it is the opinion of the Examiner that none of OP0 – OP9 corresponds to the "first clock signal" or the "second clock signal" since the Examiner has characterized those as corresponding to the recited "data signals" (see *Office Action* at 3). In other words, the Examiner has simply not addressed how *Chen* teaches or discloses a "first clock signal" or the "second clock signal" as recited in claim 1.

With continued reference to selected inconsistencies between the allegations of the Examiner and the disclosure of the cited portions of *Chen*, Applicants note that the Examiner has alleged that *Chen* discloses "...a selector (16,52) coupled to said plurality of circuit elements for sequentially selecting each of said individual data signals to generate said output data stream..." *Office Action* at 3. *Emphasis added.* In contrast with the allegations of the Examiner however, Figure 1 and col. 5, lines 16-17 of *Chen* indicate that the output of the "Clock MUX 16" (characterized by the Examiner as a "selector") is "**recovered clock 48**" ("re-timed data" is output by "Lead/Lag Phase Detector 18" – see Fig. 1). That is, the output of selector 16 is a recovered clock signal and not the multiplexed data stream recited in claim 1.

In view of the discussion set forth herein, Applicants respectfully submits that the Examiner has failed to establish that *Chen* anticipates claims 1-7 and 13, at least because the Examiner has not shown that each and every element as set forth in claim 1 is found in *Chen*, because the Examiner has not shown that the identical invention is disclosed in *Chen* in as complete detail as is contained in claim 1, and because the Examiner has not shown that *Chen* discloses all the elements of claim 1 arranged as required by that claim. Applicants thus respectfully submit that the rejection of claims 1-7 and 13 should be withdrawn.

b. claims 14-20

Applicants initially note that claim 14 has been amended to include elements similar to amended claim 1. Accordingly, claim 14 is not anticipated by *Chen* for at least the reasons explained in claim 1.

In addition, the Examiner has alleged that *Chen* discloses "...a method for multiplexing a plurality of said data signals into an output data stream..." *Office Action* at 4. However, the cited

passages make no reference to multiplexing of data but refer, instead, to a "clock multiplexer 16" and "clock phases." See, e.g., *col. 4, lines 1-3*. As noted elsewhere herein, it would thus appear that the Examiner has characterized the "clock phases" of *Chen* as corresponding to the claimed "data signals." However, *Chen* explains that "The one output signal line OP0-OP9 that does switch to a logic 1 indicates to the clock multiplexer 16 which one of the ten clock phases P0-P9 should be initially selected via the select signal lines S0-S9 as the recovered clock signal 48..." *Col. 5, lines 2-6. Emphasis added. Chen* explains further that the clock multiplexer is "...for generating a recovered clock signal." *Col. 2, lines 46-49. Emphasis added.* As well, *Chen* draws a distinction between "clock" and "data," referring to "... the embedded clock signal in the incoming data stream 36 and the recovered clock 48..." (*col. 5, lines 15-17, emphasis added*). In light of these points, Applicants submit that the apparent allegation of the Examiner that the "clock signals" of *Chen* correspond to the claimed "data" is inconsistent with the disclosure in the cited portions of *Chen*. Finally, the Examiner has not cited any portion of *Chen* as teaching or suggesting that the "Re-Timed Data" output of component 10 constitutes multiplexed data.

In view of the foregoing points, Applicants respectfully submit that the Examiner has not established that *Chen* discloses "...a method for multiplexing a plurality of data signals into an output data stream..." (Office Action at 4).

As well, the Examiner has also failed to specifically identify which portion(s) of *Chen* allegedly correspond to the claimed "transitions of said data signal." Instead, the Examiner has simply made non-specific references to various passages of *Chen*. Moreover, the allegation of the Examiner, as presently understood, that *Chen* discloses "clocking said circuit elements with said first clock signal to control said transitions of said data signal" (Office Action at 4, emphasis added) is illogical, since one of those "circuit elements" (as characterized by the Examiner), i.e., "Analog PLL 12," is the device that actually generates the clocks. Particularly, *Chen* notes that Analog PLL 12 "generates high-speed clocks for the transmit path..." *Col. 3, lines 64-66*.

In view of the discussion set forth herein, Applicants respectfully submit that the Examiner has failed to establish that *Chen* anticipates claims 14-20, at least because the Examiner has not shown that each and every element as set forth in claim 14 is found in *Chen*, because the Examiner has not shown that the identical invention is disclosed in *Chen* in as complete detail as is contained in claim 14, and because the Examiner has not shown that *Chen* discloses all the elements of claim

14 arranged as required by that claim. Applicants thus respectfully submit that the rejection of claims 14-20 should be withdrawn.

c. claims 25-27 and 30

Applicants initially note that claim 25 has been amended to include elements similar to amended claim 1. Accordingly, claim 25 is not anticipated by *Chen* for at least the reasons explained in claim 1. In addition, independent claim 25 recites a "first clock signal," "second clock signal," "an individual data signal of a plurality of data signals," and a "selector…[which generates] said output data stream." Applicants thus submit that the rejection of claim 25 is not well taken for at least the reasons set forth above in connection with the discussion of claim 1, and the attention of the Examiner is respectfully directed to such discussion. Applicants further submit that the rejection of claims 25-27 and 30 should be accordingly withdrawn.

III. Claim Rejections under 35 USC § 103

The Examiner has rejected claims 8-12, 21-24, 28 and 29 under 35 USC § 103(a) over *Chen* in view of US 6,917,660 to Song ("*Song*"). Applicants respectfully disagree.

Applicants note that by virtue of their dependence from one of claims 1, 14 or 25, each of claims 8-12, 21-24, 28 and 29 requires all the elements of one of those independent claims. As noted herein however, the Examiner has not shown that *Chen*, *Song* and/or any other reference(s), considered alone or in combination, teaches all the elements of claims 1, 14 and 25.

Applicants thus submit that the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 8-12, 21-24, 28 and 29, at least because the Examiner has not shown that the references, when combined in the allegedly obvious fashion, teach or suggest all the elements of those claims. Applicants thus respectfully submit that the rejection of claims 8-12, 21-24, 28 and 29 should be withdrawn.

CONCLUSION

In view of the foregoing, Applicants submit that all the issues raised by the Examiner have been addressed and that the pending claims are allowable. In the event that Examiner finds remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview or overcome by an Examiner's Amendment, Examiner is requested to contact the undersigned attorney.

Dated this 12th day of January, 2009.

Respectfully submitted,

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